IN THE CLAIMS:

Please cancel claims 7-24. Original claims 1-6 are listed as follows:

1. (Original) A method for fabricating a DRAM cell arrangement with vertical MOS transistors, comprising:

forming a source/drain material on a substrate;

etching trenches to form a plurality of parallel ribs having strips of the source/drain material disposed thereon, wherein the strips provide sites for a plurality of upper source/drain regions of the vertical MOS transistors;

depositing a covering layer on a floor of the trenches;

depositing a gate dielectric layer on the surfaces of the ribs;

filling the trenches, whereby gate electrodes for the vertical MOS transistors are produced on either side of the ribs;

forming a plurality of word lines over, and cross-wise with respect to, the ribs;

depositing a first auxiliary layer, capable of wafer bonding, on the plurality of word lines;

attaching a first auxiliary carrier substrate to the first auxiliary layer;

removing at least the substrate;

forming a plurality of lower source/drain regions on the ribs, wherein portions of the ribs disposed between the plurality of lower source/drain regions and the plurality of upper source/drain regions define channel regions for the vertical MOS transistors; and

forming shallow isolation trenches to isolate the plurality of lower source/drain regions.

2. (Original) The method of claim 1, further comprising forming capacitors stacked, with respect to the vertical MOS transistors, on the first auxiliary carrier substrate and in electrical contact with the plurality of lower source/drain regions of respective vertical MOS transistors.

3. (Original) The method of claim 1, further comprising:

depositing a second auxiliary layer, capable of wafer bonding, on the first auxiliary carrier substrate;

attaching a second auxiliary carrier substrate to the second auxiliary layer;

removing the first auxiliary carrier substrate and the first auxiliary layer;

forming metal bit lines on the second auxiliary carrier substrate for making direct electrical contact with the plurality of upper source/drain regions.

4. (Original) The method of claim 1, wherein the substrate and ribs are components of an SOI substrate comprising a buried oxide layer and further comprising removing the buried oxide layer prior to forming the plurality of lower source/drain regions on the ribs.

5. (Original) The method of claim 1, wherein forming the plurality of upper and lower source/drain regions comprises implanting doping ions.

6. (Original) The method of claim 1, wherein etching the trenches is done using lithographically produced mask patterns.

7-24. (Canceled)

Please add the following new claims:

25. (New) A DRAM cell arrangement with vertical MOS transistors, comprising:

a plurality of upper source/drain regions of the vertical MOS transistors formed by etching trenches in a source/drain material formed on a substrate to form a plurality of parallel ribs having strips of the source/drain material disposed thereon;

a covering layer deposited on a floor of the trenches;

a gate dielectric layer deposited on the surfaces of the ribs;

a plurality of gate electrodes for the vertical MOS transistors formed on either side of the ribs by filling the trenches;

a plurality of word lines formed over, and cross-wise with respect to, the ribs;

a first auxiliary layer, capable of wafer bonding, deposited on the plurality of word lines;

a first auxiliary carrier substrate attached to the first auxiliary layer;

a plurality of lower source/drain regions formed on the ribs after removal of the substrate, wherein portions of the ribs disposed between the plurality of lower source/drain regions and the plurality of upper source/drain regions define channel regions for the vertical MOS transistors; and

a plurality of shallow isolation trenches formed to isolate the plurality of lower source/drain regions.

26. (New) The DRAM cell arrangement of claim 25, further comprising:
a plurality of capacitors stacked, with respect to the vertical MOS transistors, on the first auxiliary carrier substrate and in electrical contact with the plurality of lower source/drain regions of respective vertical MOS transistors.

27. (New) The DRAM cell arrangement of claim 25, further comprising:

a second auxiliary layer, capable of wafer bonding, deposited on the first auxiliary carrier substrate;

a second auxiliary carrier substrate attached to the second auxiliary layer; and

a plurality of metal bit lines formed, after removal of the first auxiliary carrier substrate and the first auxiliary layer, on the second auxiliary carrier substrate for making direct electrical contact with the plurality of upper source/drain regions.

28. (New) The DRAM cell arrangement of claim 25, wherein the substrate and ribs are components of an SOI substrate comprising a buried oxide layer.

29. (New) The DRAM cell arrangement of claim 28, wherein the buried oxide layer is removed prior to forming the plurality of lower source/drain regions on the ribs.

30. (New) The DRAM cell arrangement of claim 25, wherein the plurality of upper and lower source/drain regions are formed by implanting doping ions.

31. (New) The DRAM cell arrangement of claim 25, wherein the trenches are etched utilizing lithographically produced mask patterns.